AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims

1. – 13.   (Canceled)

14.   (Previously Presented) A computer system, comprising:

a host processor;

a shadow processor coupled to the host processor, the shadow processor adapted to control interrupts received from peripherals connected to a computer processor system;

the host processor in communication with an external bus via an external bus interface, the external bus adapted to transfer data to and from a main processor and at least one memory device;

a memory controller within the host processor for controlling data access to the at least one memory device;

an execution unit for controlling the memory controller and a main processor;

an arithmetic logic unit and a plurality of registers within the host processor;

the memory controller, arithmetic logic unit and registers and host processor being inter-communication via at least one internal bus;

the host processor adapted to process a first set of instructions;

the shadow processor adapted to process a second set of instructions, the second set of instructions being a subset of the first set of instructions; and

the shadow processor adapted to receive control signals and to process instructions in dependence upon those control signals independently of the host processor means.

15. (Previously Presented) The computer system of Claim 14, in combination with a main processor.

16. (Previously Presented) The computer system of Claim 15, further comprising the shadow processor being coupled to the main processor.

17. (Previously Presented) The computer system of Claim 14, adapted to hold the host processor in a low power inactive mode while the shadow processor is processing a second set of instructions.

18. (Previously Presented) The computer system of Claim 14, further comprising an interrupt controller within the shadow processor, adapted to receive interrupt signals via at least one interrupt input.

19. (Previously Presented) The computer system of Claim 18, further comprising the interrupt controller being coupled to at least one peripheral via at least one peripheral bus.

20. (Previously Presented) The computer system of Claim 14, the shadow processor further comprising registers which correspond to selected registers of the host processor.

21. (Previously Presented) The computer system of Claim 20, wherein the shadow processor further includes an execution unit, code memory and data memory.

22. (Previously Presented) The computer system of Claim 21, wherein the shadow processor is adapted to process a selected subset of the instructions from which the host processor operates, and these instructions are stored in the code memory.

23. (Previously Presented) The computer system of Claim 22, wherein the shadow processor is adapted to access to the memory of the host processor by way of a memory controller which interfaces with the external bus by way of the host external bus interface.

24. (Previously Presented) The computer system of Claim 23, further comprising:

a host interrupt controller adapted to couple the host processor execution unit to the shadow processor execution unit;

a register bridged unit adapted to couple the at least one register of the host processor to the at least one register of the shadow processor.

25. (Previously Presented) The computer system of Claim 24, wherein the host interrupt controller is adapted to allow the shadow processor to issue an interrupt to the host processor in order to cause a change in task execution.

26. (Previously Presented) The computer system of Claim 25 wherein the interrupt to the host processor uses a host interrupt protocol and indicates the source of the interrupt as a vector programmed by the shadow process related to the new task required.